

**Revision : 1.22**

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23	ATX, FRONT PANEL
24	VCORE(RT8868+RT9612)
25	POWER SEQUENCE,EUP

[illegible]

**Model Name:GA-78LMT-S2**

## Component value change history

**Version: 1.22**

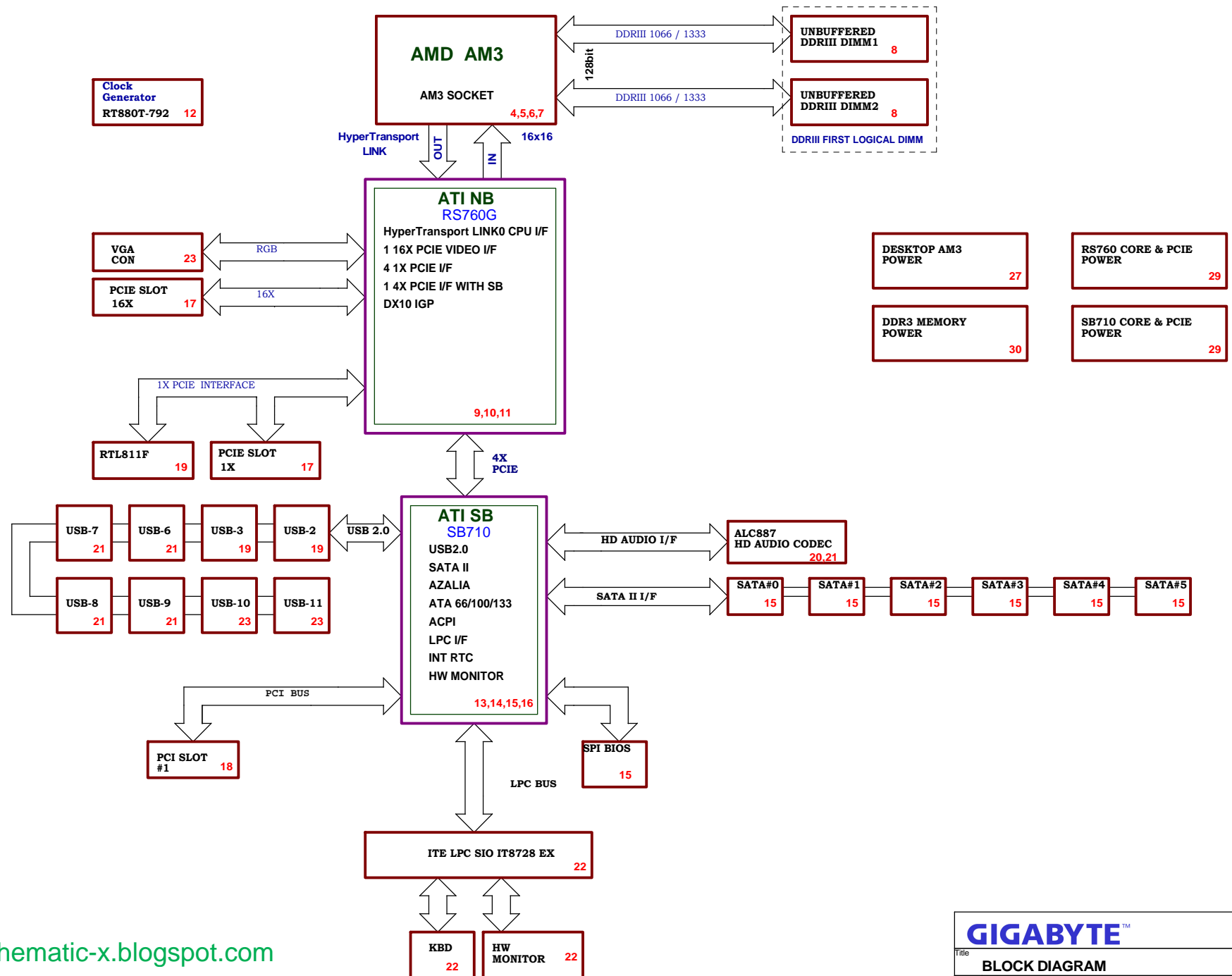
**P-Code: U99098-0**

[illegible]

### Circuit or PCB layout change for next version

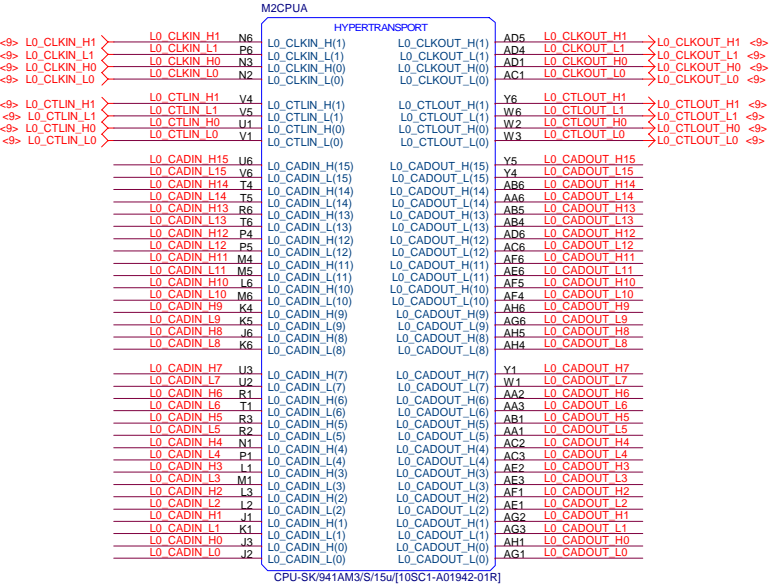
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# RS780L CUSTOMER DESKTOP DESIGN



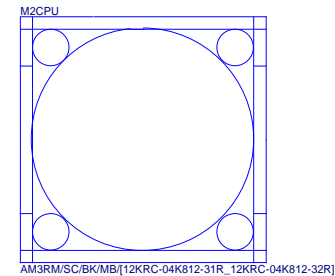
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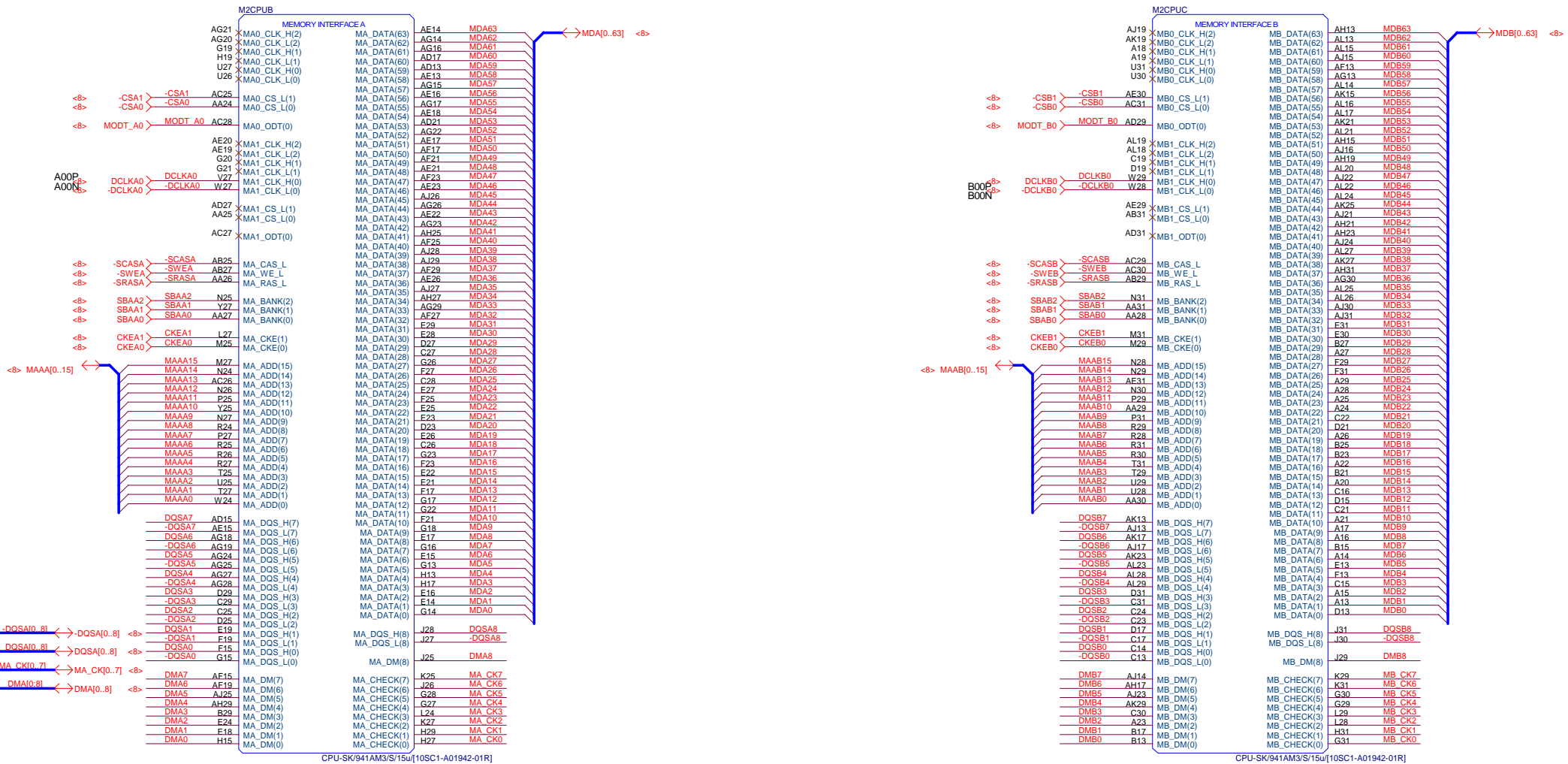
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L0\_CADOUT\_H[0..15] <L0\_CADOUT\_H[0..15] <9>



CPU\_VDD\_RUN = VCORE  
CPU\_VDDA\_RUN = VDDA25  
VLDT\_RUN = VCC12\_HT  
CPU\_VDDIO\_SUS = DDR18V  
CPU\_VTT\_SUS = DDRVTT

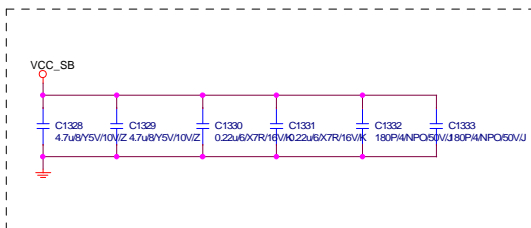
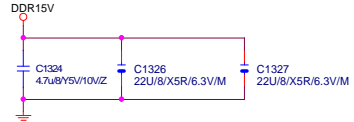
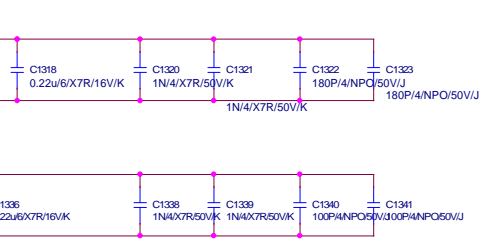
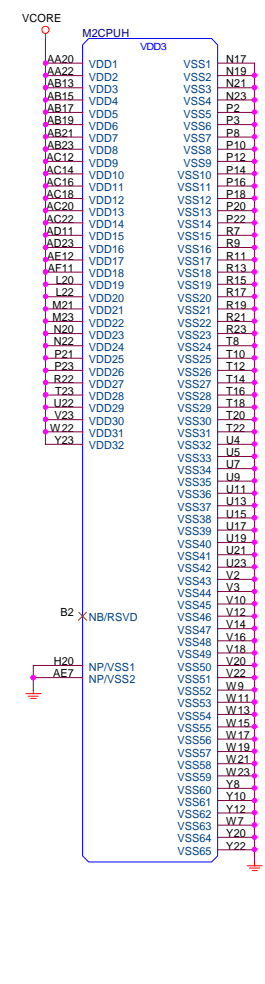
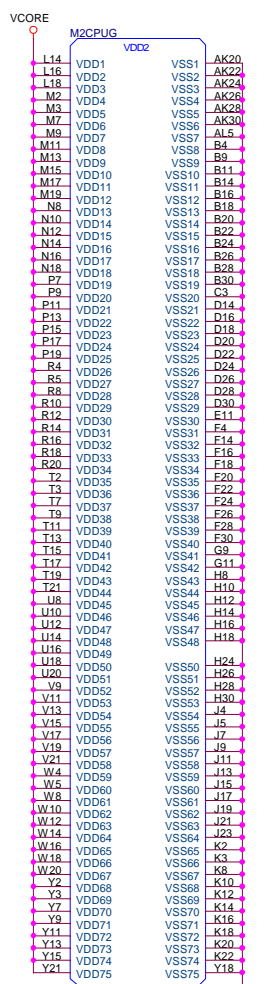
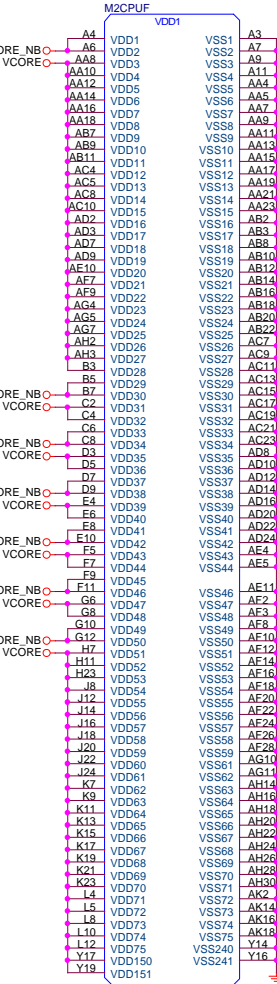
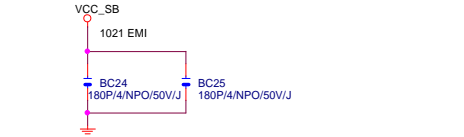
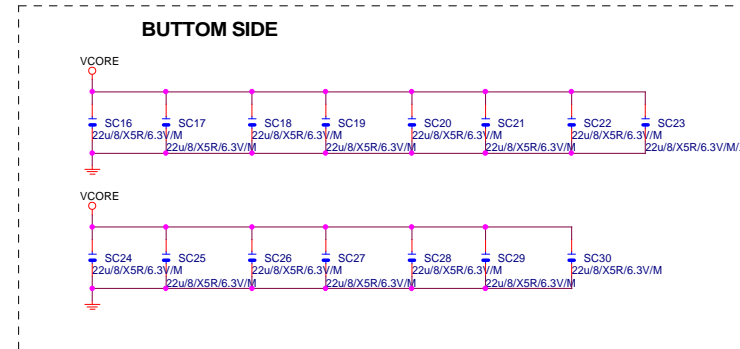
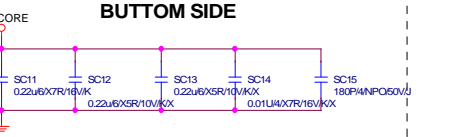
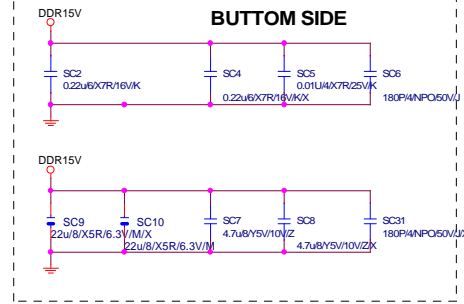
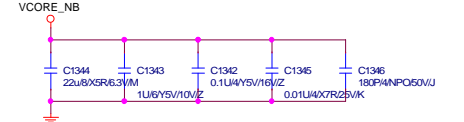
VLDT\_A = VCC12\_HT  
VLDT\_B = HT12B





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L0\_CADIN\_L[0..15] <L0\_CADIN\_L[0..15] <4>  
L0\_CADIN\_H[0..15] <L0\_CADIN\_H[0..15] <4>  
L0\_CADOUT\_L[0..15] <L0\_CADOUT\_L[0..15] <4>  
L0\_CADOUT\_H[0..15] <L0\_CADOUT\_H[0..15] <4>

PART 1 OF 6

HYPER TRANSPORT CPU  
I/F



RS780L/FCBGA528/A13[10HB1-06760G-20R]

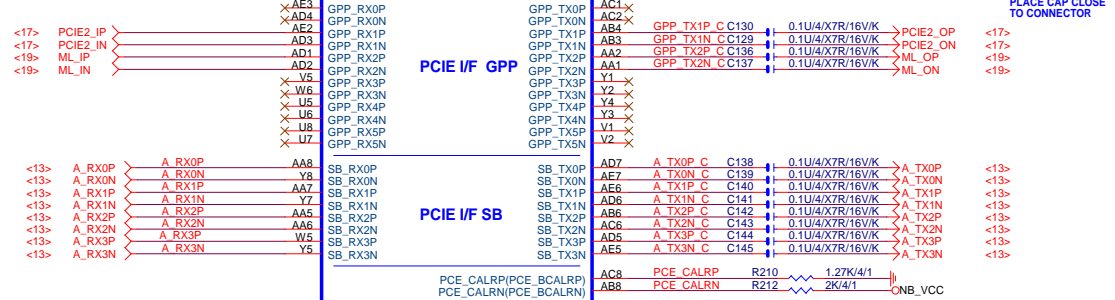
EXP\_A\_RXP[0..15] >>EXP\_A\_RXP[0..15] <17>  
EXP\_A\_RXN[0..15] >>EXP\_A\_RXN[0..15] <17>  
EXP\_A\_TXP[0..15] >>EXP\_A\_TXP[0..15] <17>  
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PART 2 OF 6

PCI E I/F  
GFX

PCI E I/F  
GPP

PCI E I/F  
SB



RS780L/FCBGA528/A13[10HB1-06760G-20R]

# RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX\_CAL, place close to pin C8

RS740\_DFT\_GPIO1 R272 150/4/1

Note: for RX780, R217 (RX780\_DFT\_GPIO1) to 3K accordingly

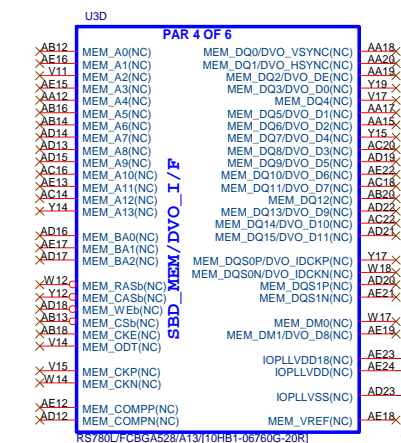
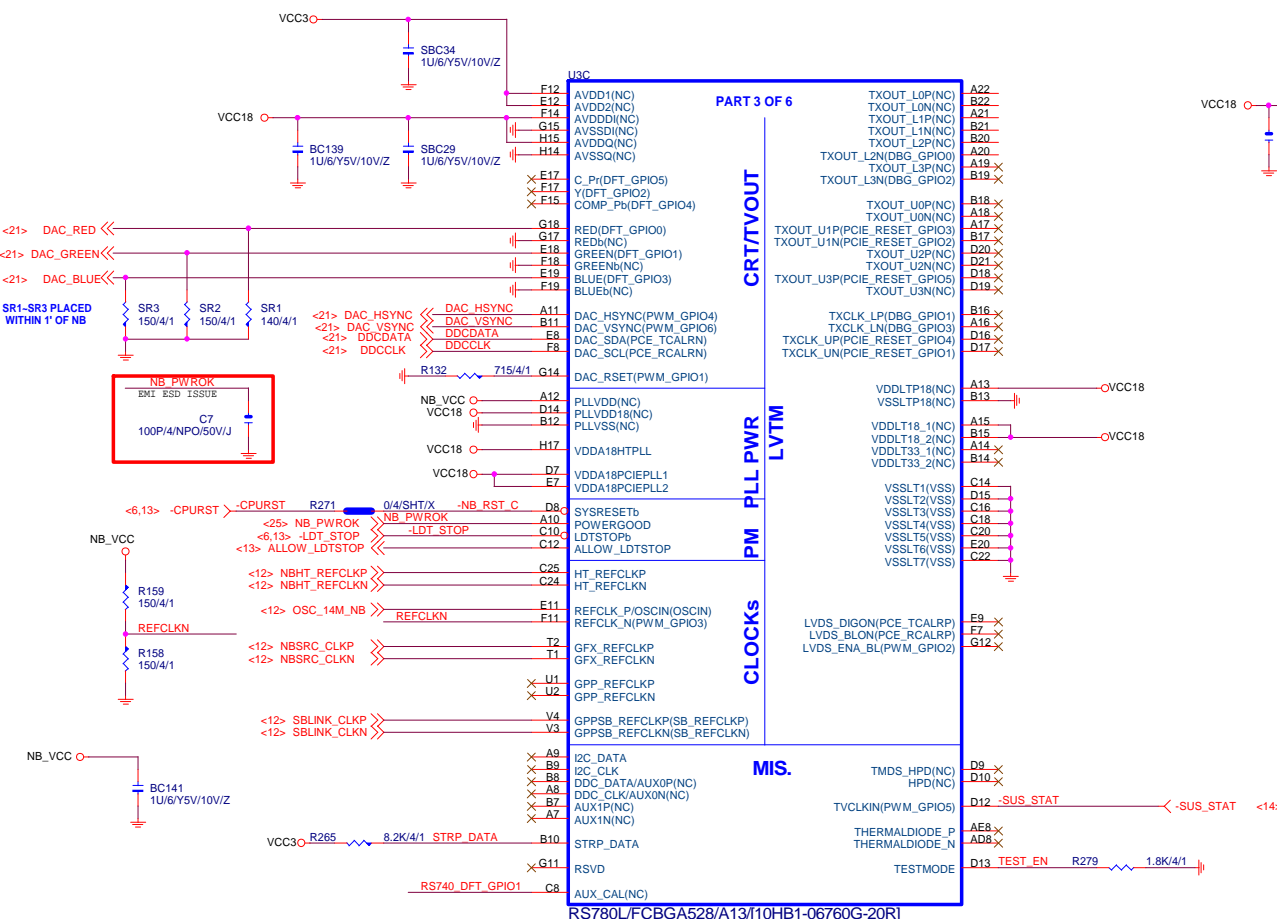
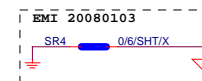
<21> DAC\_VSYNC << R276 3K/4/1 >> VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly  
R912 (RX780\_DFT\_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly  
R913 (RX780\_DFT\_GPIO4)  
R218 (RX780\_DFT\_GPIO3)  
R911 (RX780\_DFT\_GPIO2)

<21> DAC\_HSYNC << R285 3K/4/1 >> VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly  
R219 (RX780\_DFT\_GPIO0)





PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLTP18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDLTP33	+3.3V	NC	NC



- 
- 9LPRS482 / RTM880T-792**
- RTM880T-792/S**
- RS740 Stuff 330ohm**  
**RS780 Stuff 150ohm**
- Star**

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

**SEL_HTT66/REF0		OUT 3.3V 14.318MHz REF output.
IN	Low	100MHz differential HT clock, (Internal 120KΩ pull-down)
	High	66MHz 3.3V single ended HT clock.

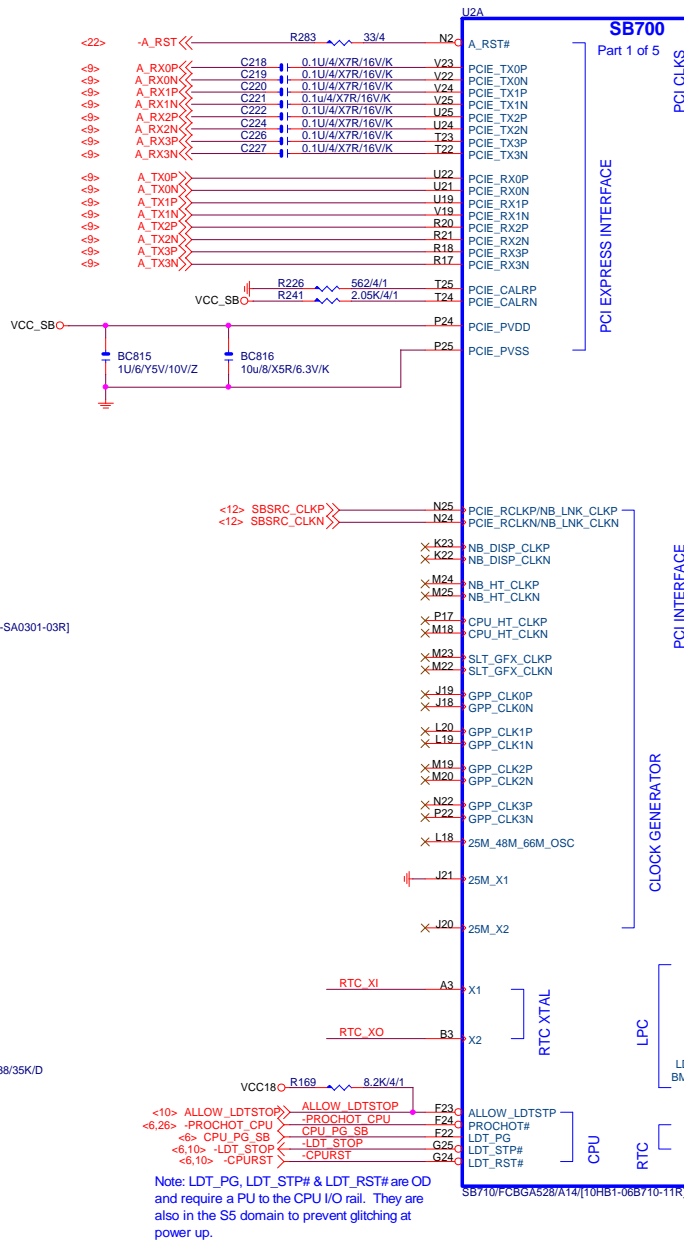
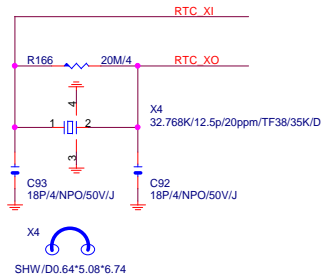
NB CLOCKS		RS740	RX780	RS780	
HT_REFCLKP	60M (SEI0E)	100M DIFF	100M DIFF		
HT_REFCLKN	NC	100M DIFF	100M DIFF		
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)		100M DIFF
REFCLK_N	NC	NC	vref		100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF		
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)		
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF		

\* the GFX\_REFCLK input is required for all cases

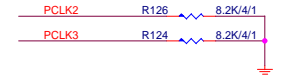
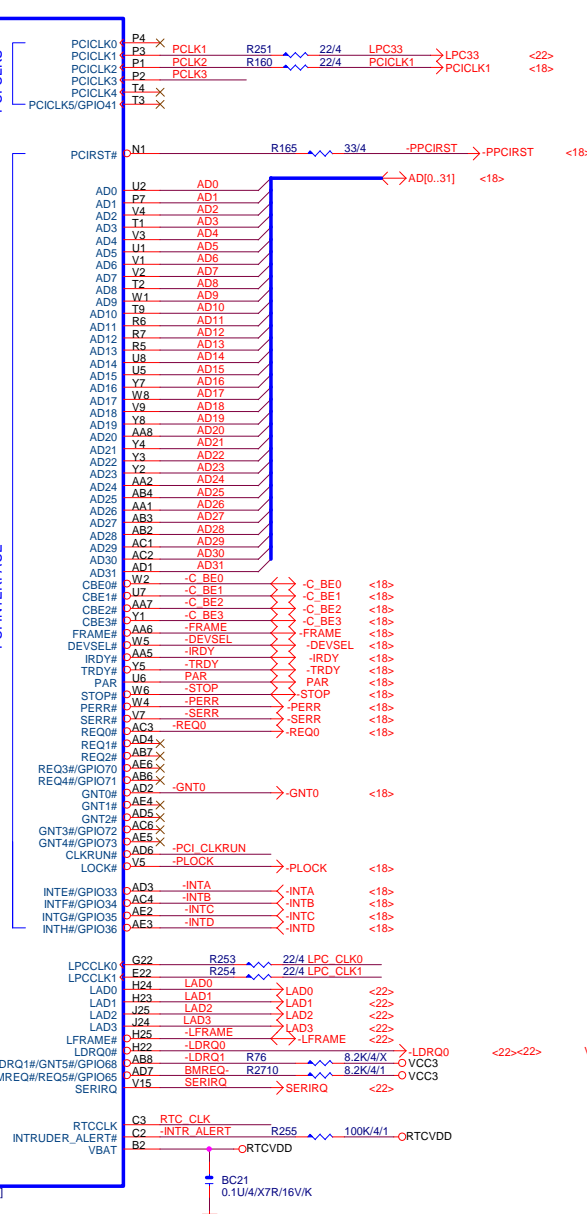


Diagram of a square loop with a magnetic field vector  $B$  pointing upwards. The top-left corner is labeled "SB\_HS".

SB\_HS[12SP2-SA0301-01R\_12SP2-SA0301-02R\_12SP2-SA0301-03R]



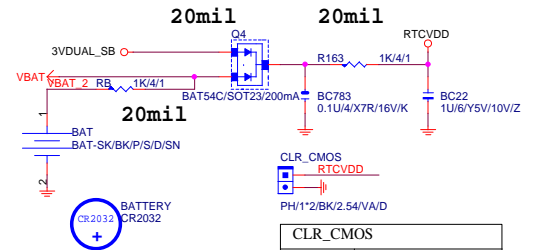
Note: LDT\_PG, LDT\_STP# & LDT\_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.



	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

BIOS after boot setting  
EC AOD-ACC

	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED	CLKGEN ENABLED
PULL LOW	AOD Extreme IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT



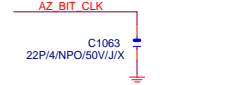
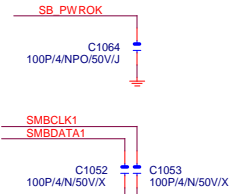
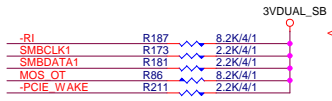
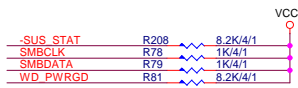
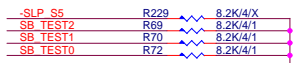
**NOT ADD ICT FOR RTCVDD PIN**

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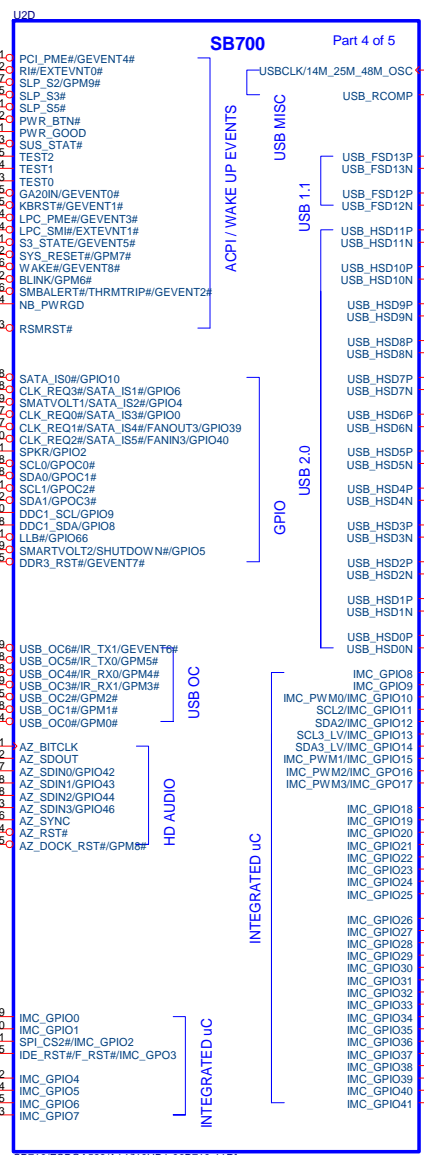
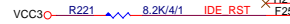
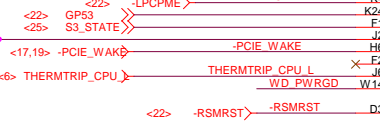
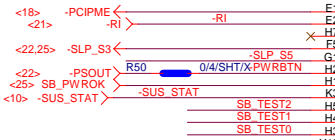
ATI SB710 PCIE/PCI/CPU/LPC

Size	Document Number	Rev
Custom	<b>GA-78LMT-S2</b>	<b>1.22</b>

Date: Thursday, July 04, 2013 Sheet 13 of 27



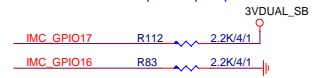
**AZ\_RST#**  
 PULL HIGH ENABLE PCI MEM BOOT  
 PULL LOW DISABLE PCI MEM BOOT  
 DEFAULT



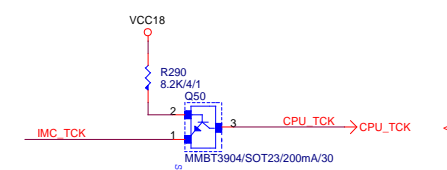
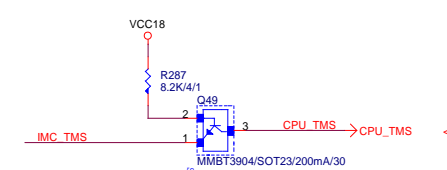
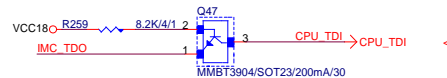
SB710/FCBGA528/A14(10HB1-06B710-11R)

USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

either HWM inputs or PWR\_GD signals can be used for power-up sequencer



**IMC\_GPIO17** **IMC\_GPIO16**  
 ROM TYPE:  
 H, H = Reserved  
 H, L = SPI ROM DEFAULT  
 L, H = LPC ROM  
 L, L = FW ROM





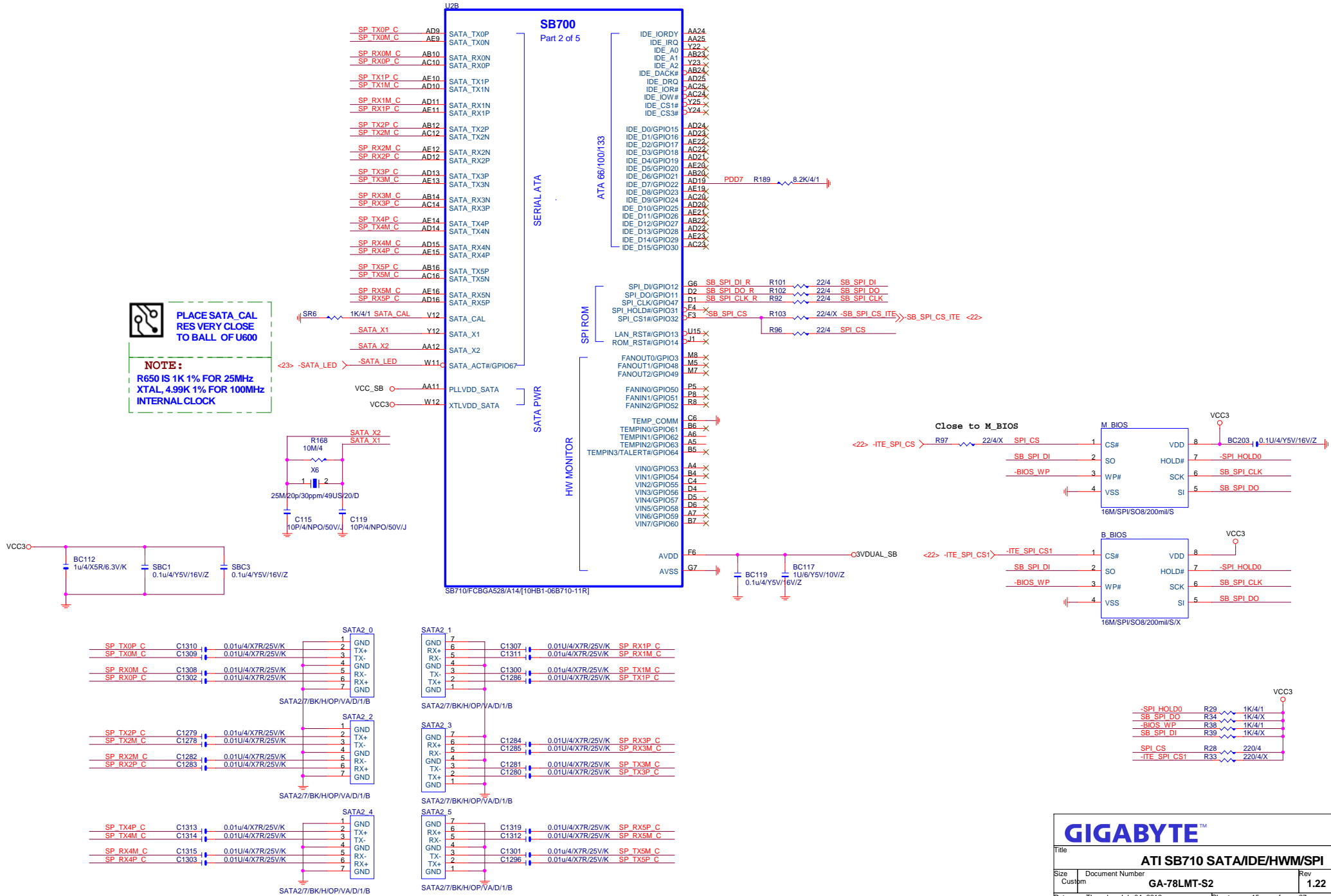
PLACE SATA AC COUPLING  
CAPS CLOSE TO SB600



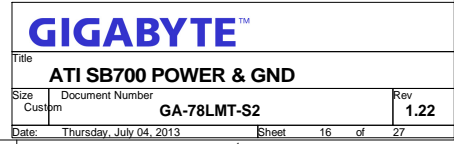
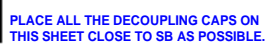
PLACE SATA CAL  
RES VERY CLOSE  
TO BALL OF U600

NOTE:

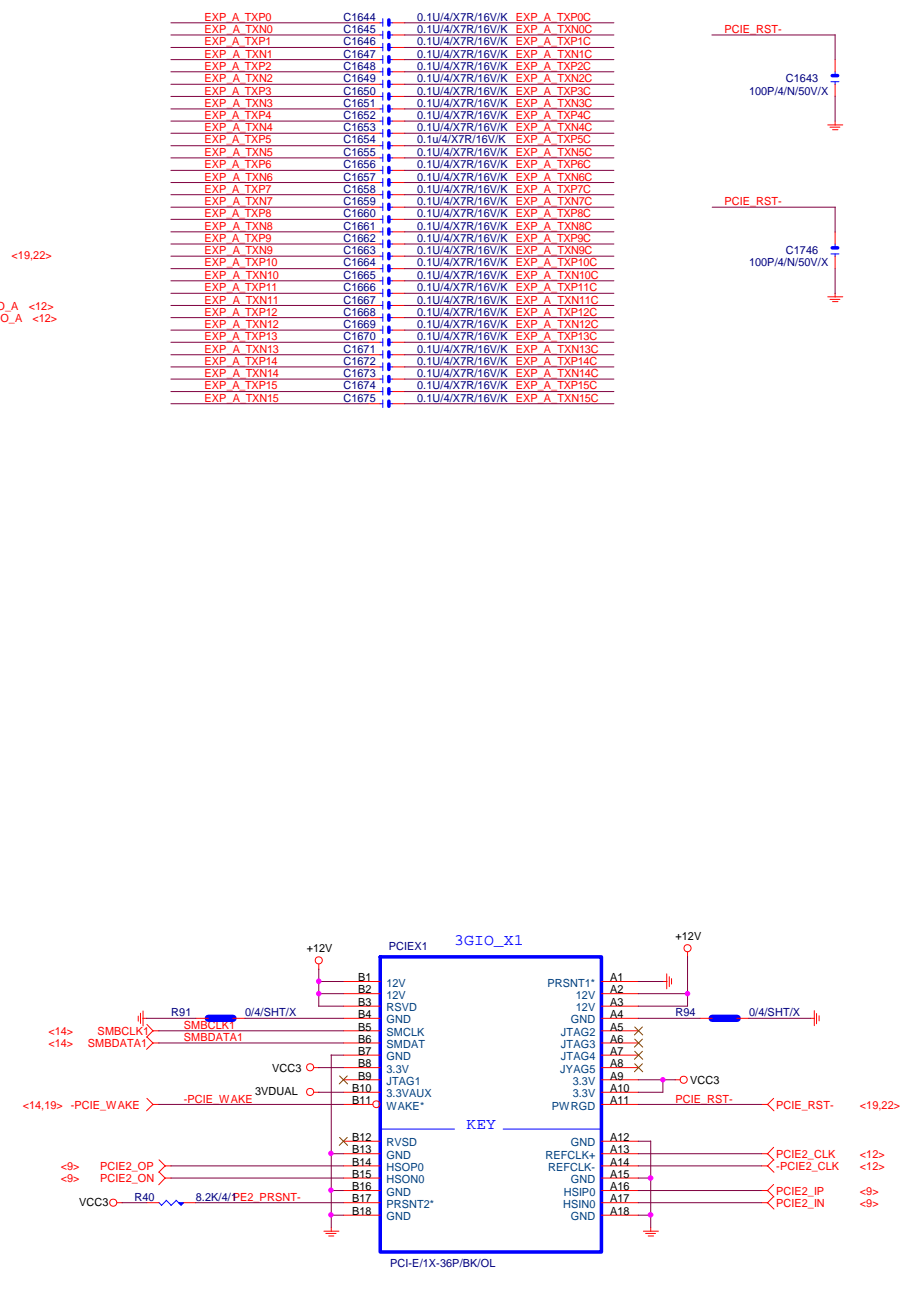
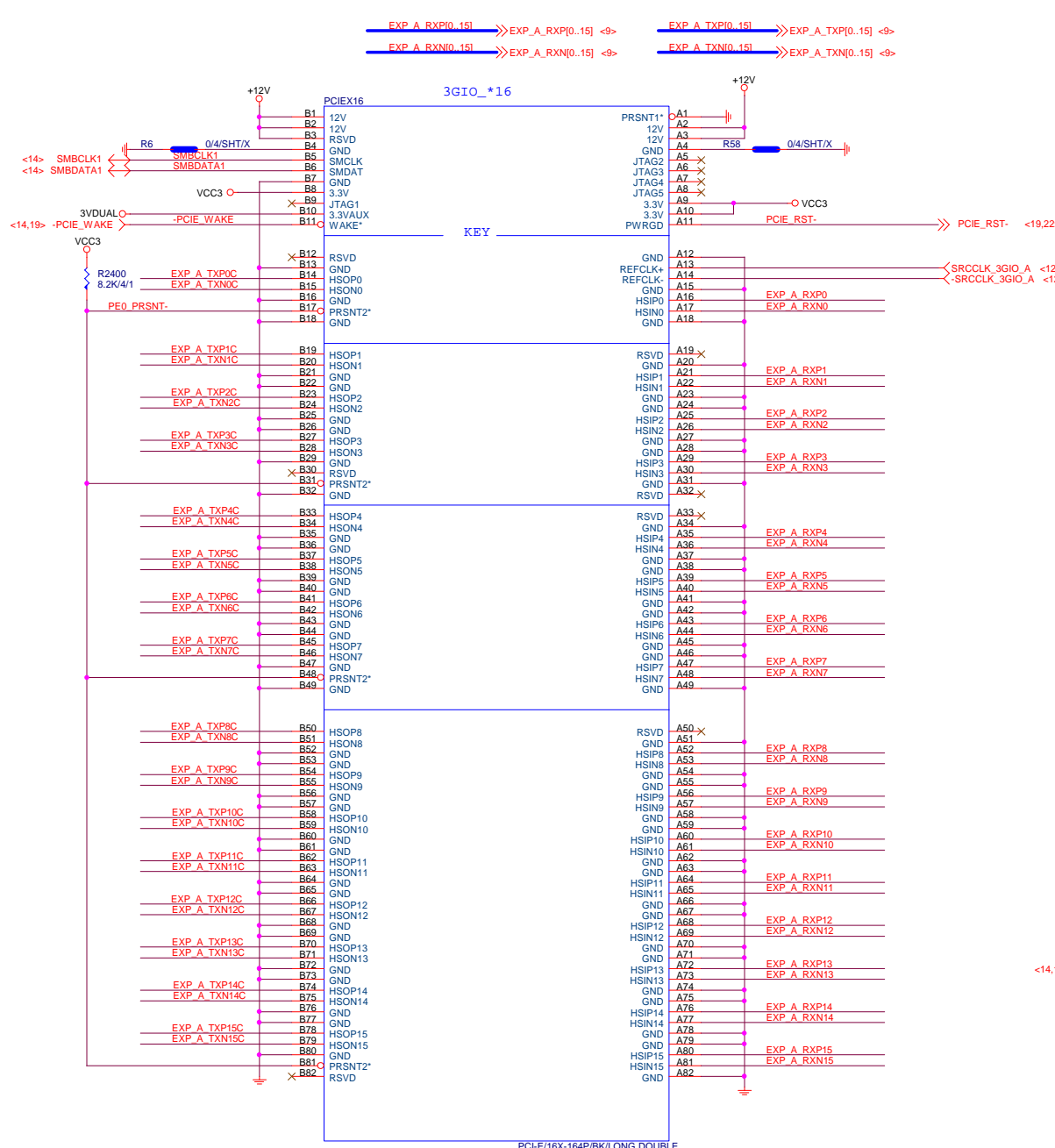
R650 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK









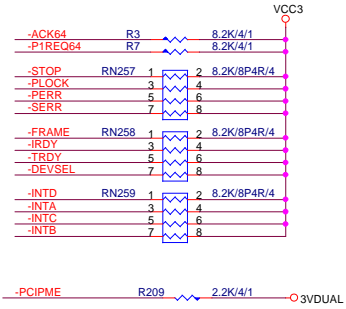
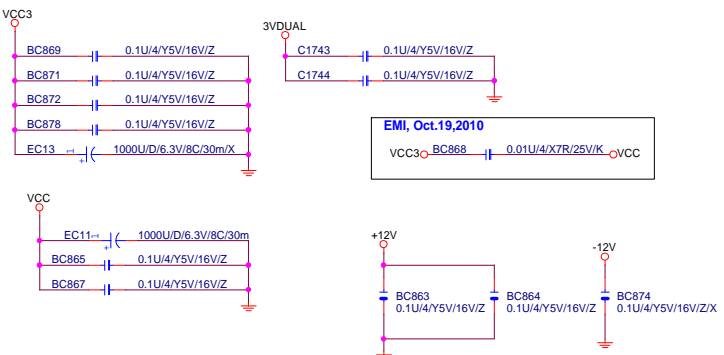
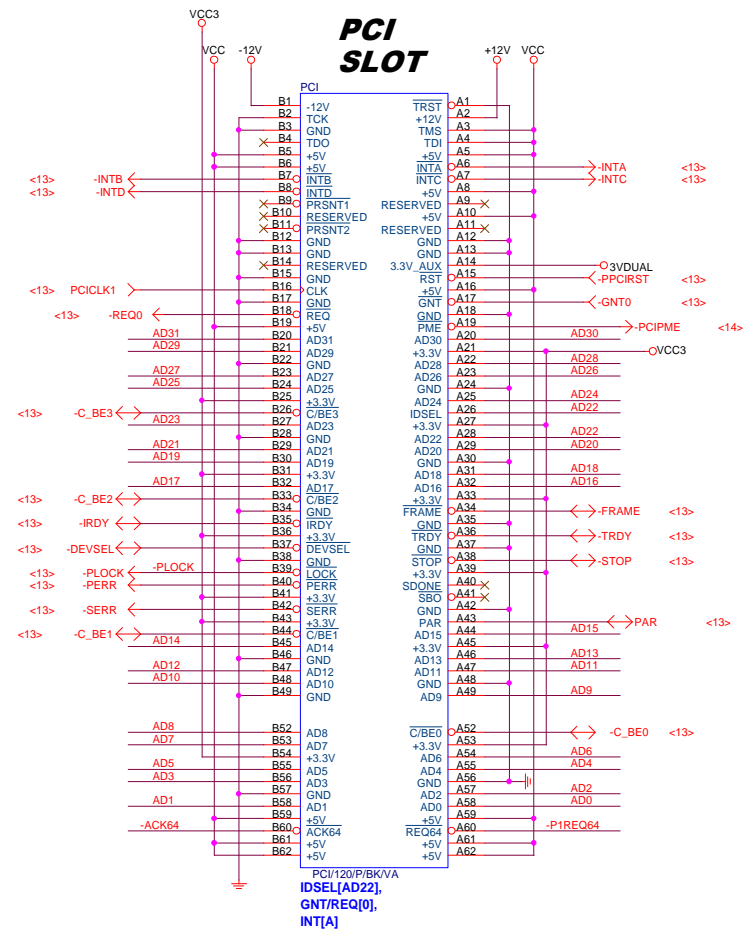


# PCI SLOT 1,2

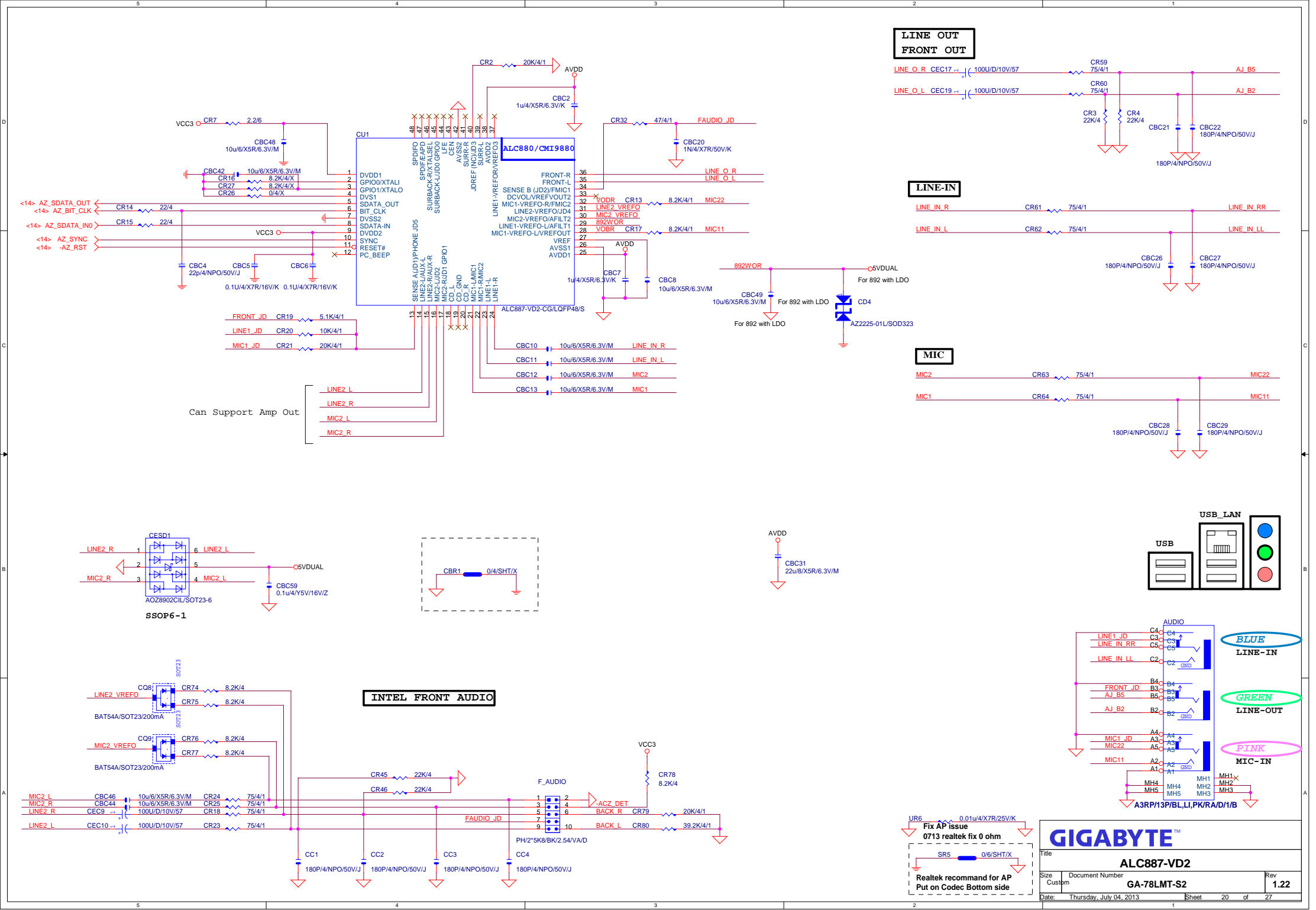
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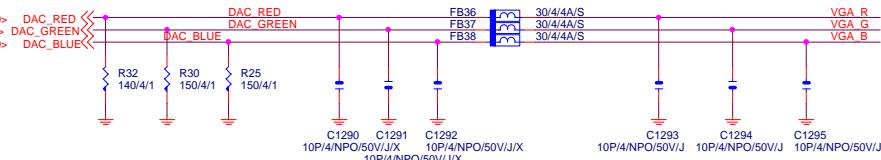
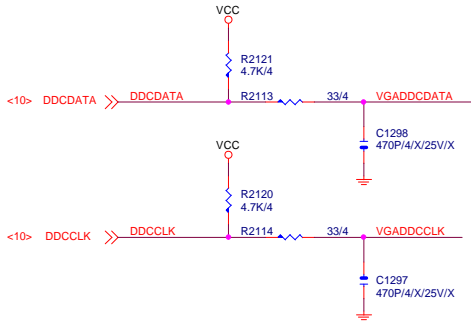
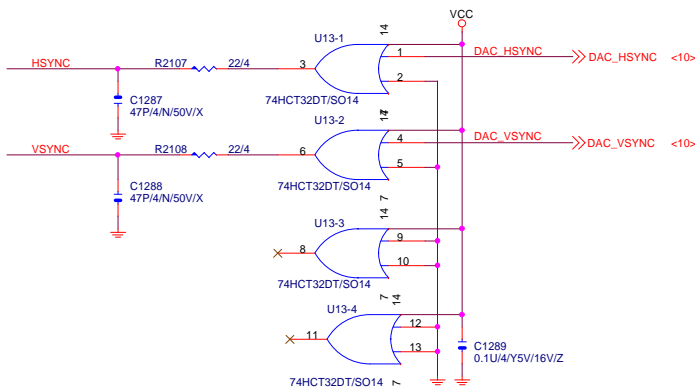
PCICLK1 BC861 10P/4/N/50V/X

-PPCIRST C1745 100P/4/N/50V/X

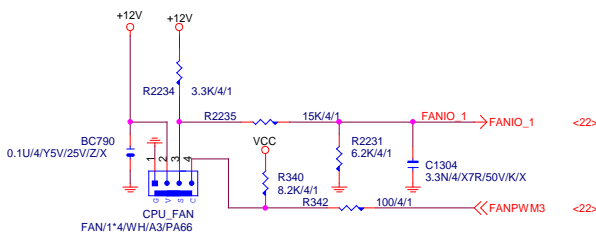




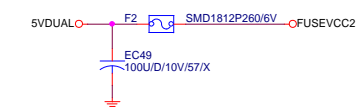
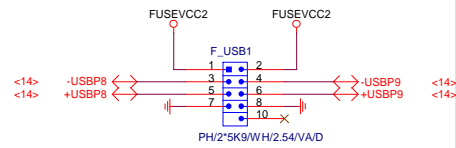
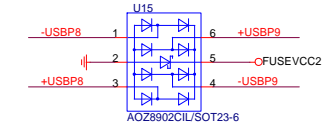
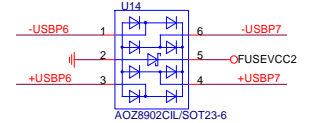
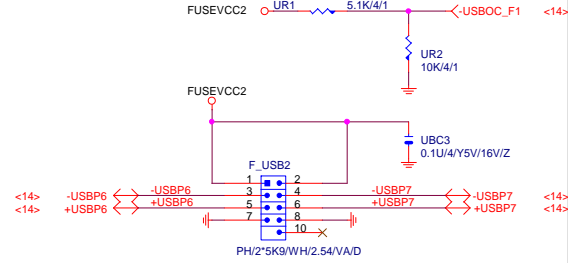
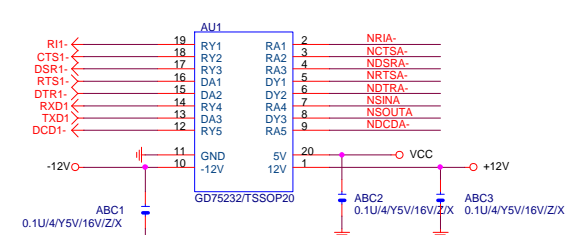
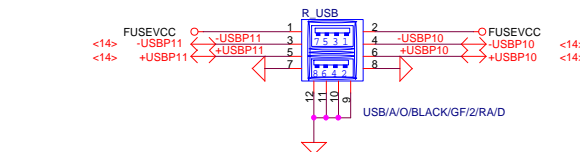
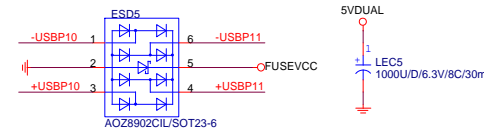
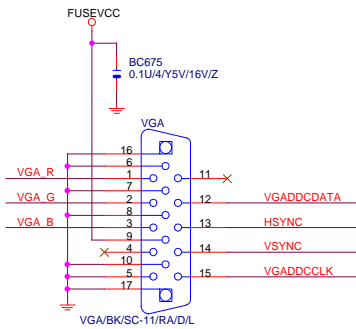
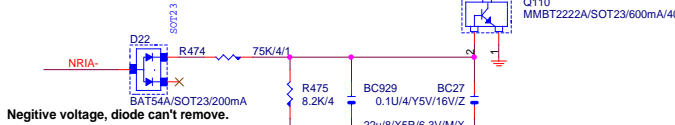
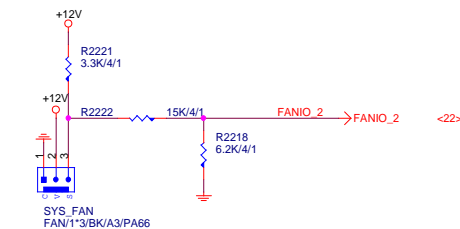


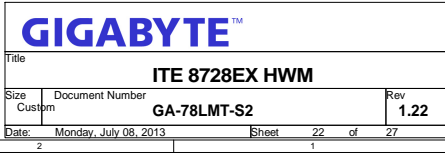


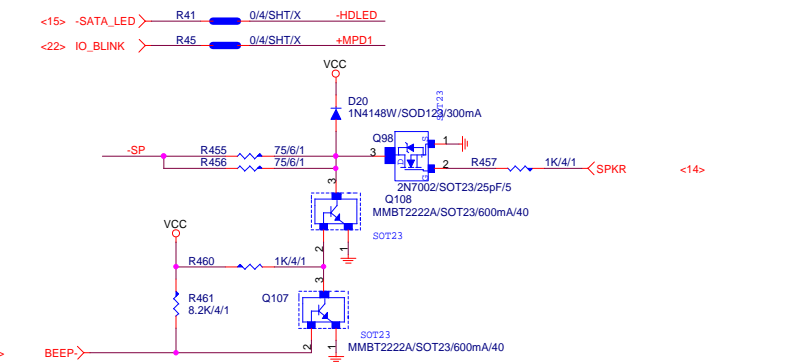
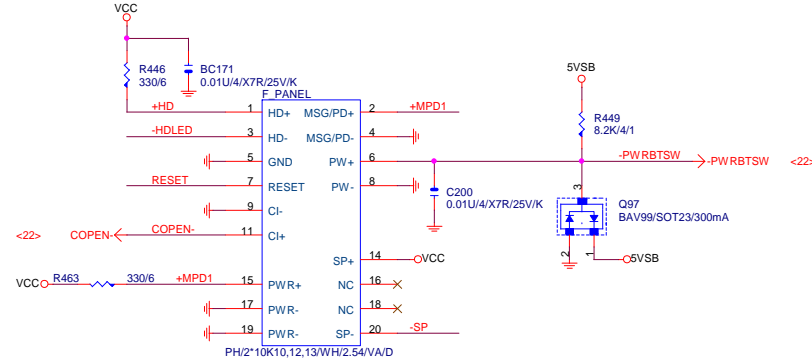
## CPU\_FAN



## SYSTEM FAN







### ATX POWER CONNECTOR

